APPLICATION FOR
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IN THE NAME OF

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FOR

MEMORY MODULE AND MEMORY COMPONENT BUILT-IN SELF TEST

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TITLE OF THE INVENTION

MEMORY MODULE AND MEMORY COMPONENT BUILT-IN SELF TEST

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates generally to memory systems, and more specifically, to memory modules and memory components, such as a memory device or a memory buffer, having built-in self test functionality.

2. Discussion of the Related Art

Integrated circuit devices such as random access memories (RAMs) usually undergo device verification testing during manufacture. Typically, such verification tests are designed to detect both static and dynamic defects in a memory array. Static defects include, for example, open circuit and short circuit defects in the integrated circuit device. Dynamic defects include defects such as weak pull-up or pull-down transistors that create timing sensitive defects.

A specialized integrated circuit device tester is normally employed to perform manufacturing verification tests. For example, such an integrated circuit device tester may be used to perform read/write verification cycle tests on the memory array. Relatively low-speed (e.g., 20 MHz), low-cost integrated circuit device testers are usually sufficient for detecting static defects in the memory array. However, extremely expensive integrated device testers are needed to detect dynamic defects in very high-speed memory arrays. Such expensive high-speed integrated circuit testers increase the overall manufacturing costs for such devices. In addition,

for integrated circuit devices that include large memory arrays, the cycle time required to perform such read/write tests increases in proportion to the size of the array.

Attempts to overcome some of the difficulties associated with testing integrated circuit devices have included implementing built-in self-test (BIST) circuitry. For example, an integrated circuit cache memory array may contain circuitry to perform a standard static random access memory (SRAM) 13N March test algorithm on the memory array. A state machine is typically used to generate the 13N March test algorithm along with circuitry to sample data output and to generate a signature of the results. The signature is then compared against an expected value to determine whether defects exist in the memory array. Such BIST circuitry usually enables high-speed testing while obviating expensive high-speed testers.

Unfortunately, these BIST routines have generally only been able to apply a preprogrammed test sequence on the memory array. As the process of manufacturing such a memory array evolves, manufacturing test engineers typically develop improved strategies for detecting both static and dynamic defects in the memory array.

Moreover, such improved strategies for detecting defects can only be applied to testing that occurs while the device is placed in an expensive integrated circuit device tester. Therefore, engineers have been unable to achieve the benefits of improved test strategies without the use of an expensive tester, or without redesigning the integrated circuit device. Because of the advances in memory technology, and particularly in the area of narrow high-speed buses, which typically run at speeds of about 1.6 GHz, for use with dynamic random access memory devices (DRAMs), it is very expensive to obtain a high-speed tester capable of testing a memory module or a memory component at such high operating frequencies. Therefore, the added use of expensive high-speed hardware testers increases the time required to ascertain hardware failures,

not to mention greatly increasing the overall manufacturing cost of these memory modules and memory components.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 illustrates a memory module having built-in self test according to an embodiment of the present invention; and

Fig. 2 illustrates a memory component having built-in self test according to an embodiment of the present invention.

DETAILED DESCRIPTION

Fig. 1 illustrates a memory module having built-in self test (BIST) according to an embodiment of the present invention. By utilizing the memory module 100 of Fig. 1, an expensive external high-speed tester is not required to test the memory module 100. The memory module 100 is configured so as to utilize BIST without any external equipment.

The memory module 100 shown in Fig. 1 utilizes a set of buffers 130, 140, 150 in order to provide an interface with a processor component, such as a memory controller (not shown), which may be operating at a different voltage and/or frequency than the memory devices 110, 120, such as dynamic random access memory (DRAM) devices. In the embodiment of Fig. 1, a three-buffer configuration is utilized for the memory module 100: two data buffers 1st 130, 2nd 140, and an address and command buffer 150. However, the 1st and 2nd data buffers 130, 140 and the address and command buffer 150 may be incorporated into a single buffer device, or additional buffer components may be utilized as well.

In one embodiment, the built-in self test (BIST) logic and circuitry are incorporated with the address and command buffer 150. The address and command buffer preferably includes an address and command generator 154 to generate the address and commands and the test data to be transmitted to the memory devices 110, 120 for testing. However, instead of generating the test data, the BIST logic may utilize existing data extracted from the memory controller off of the data bus as the test data as well. Along with generating the test data, the address and command generator 154 also generates compare test data, which is used to compare the test data read from the memory devices 110, 120, with the test data (which is identical to the compare test data) initially transmitted from the address/command generator 154 to the memory devices 110,120 for storage.

In one embodiment, the test data generated by the address/command generator 154 is transmitted to the memory devices 110, 120 for storage therein. Then, the test data stored (written) in the memory devices 110, 120 are read from the memory devices 110, 120 and compared with the compare test data, which is identical to the test data, also generated by the address/command generator 154. A comparator 145, such as an "exclusive OR" (XOR) comparator, may be provided in each one of the data buffers 130,140 to compare the test data read from the memory devices 110, 120 with the compare test data provided by the address/command generator 154. A determination of whether the comparison is a match or a failure is made by the comparator 145, and a result then is preferably transmitted to a test result/status register 156, that may be provided within the address and command buffer 150. The test result/status register 156 may then provide a test status or result signal to an external device, such as a memory controller. The test status/result signal generated by the test result/status register 156 may utilize a two-bit packet, indicating, for example, the following states: BIST not

enabled (00); BIST executing (01); BIST failed (10); and BIST passed (11). Although Fig. 1 illustrates a memory module 100 having two memory devices 110, 120, the memory module 100 is not limited to only two memory devices, and any suitable number may be used.

Additionally, rather than using a high-speed clock signal to perform testing, the memory module 100 may use a slow speed clock signal, generating just one clock, and using a clock multiplier 152 within the address and command buffer 150 to multiply and distribute the clock signal to the memory devices 110, 120. Accordingly, by utilizing the memory module 100 illustrated in Fig. 1, the memory module 100 may be tested independently of other systems, and expensive high-speed testers are not required to test the memory devices 110,120 and their connections within the memory module 100 itself.

Fig. 2 illustrates a memory component having BIST according to an embodiment of the present invention. As illustrated in Fig. 2, BIST logic may be provided completely within a single memory component, such as a buffer 210 and a memory device 220. That is, each memory component may be taken independently of any other component and tested on its own. The buffer 210 may be an address and command buffer 150, or a data buffer 130, 140, as discussed above with respect to Fig. 1.

The BIST logic includes a controller 260 to perform the BIST operations. The controller 260 preferably receives a clock signal, and also provides test result signals from the memory component, such as a buffer 210 or a memory device 220. The controller 260, like the address and command generator 154 of Fig. 1, is adapted to generate test data and compare test data to test the functional logic or memory array 250 (depending on the type of memory component, e.g., a buffer or memory device) of the buffer component 210, or memory device 220. The test data is preferably provided to the functional logic or memory array 250, which is then

transmitted to an input/output interface 230, 240. The test data may also be transmitted directly to the input/output interface 230, 240 from the controller 260 to test the input/output interface 230, 240.

The input/output interface 230, 240 is configured with a loopback so that the test data may be directed back from an input/output connection to a compare register 270 to compare the test data from the input/output interface 230, 240, and ultimately, the functional logic or memory array 250. The controller 260 is adapted to generate and provide compare test data to the compare register 270 so that the compare register 270 may compare the test data received from the input/output interface 230, 240 with the compare test data to determine whether there was a match, and whether the test was successful. Accordingly, the compare register 270 makes a determination regarding the results of the test, and the test results are reported, preferably by the controller 260. The compare register 270 and the controller 260 may be embodied within a single device or a common circuit.

Therefore, by having memory components such as a buffer 210 and a memory device 220 with BIST, localized self-testing may be performed after the buffer 210 and the memory device 220 is manufactured. However, component-level built-in self test may be performed at various stages of manufacture and packaging, including at the wafer probe stage, during post-packaging, and even during post-assembly. Accordingly, the memory components 210, 220 of Fig. 2 may be tested independently of other components, and expensive high-speed testers are not required to test the memory components 210, 220.

While the description above refers to particular embodiments of the present invention, it will be understood that many modifications may be made without departing from the spirit thereof. The accompanying claims are intended to cover such modifications as would fall within

the true scope and spirit of the present invention. The presently disclosed embodiments are therefore to be considered in all respects as illustrative and not restrictive, the scope of the invention being indicated by the appended claims, rather than the foregoing description, and all changes that come within the meaning and range of equivalency of the claims are therefore intended to be embraced therein.